Attorney Docket No. 14950U501

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In the Application of:	)
	)
MPR	)
	)
U.S. Serial No. 10/606,216	)
	)
Filed: 6/25/2003	)
	)
Group Art Unit: 2621	)
	)
Confirmation No.: 3721	)

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Sir:

This appeal is an appeal of the Final Office Action of 7/25/08. A Notice of Appeal was filed on 10/21/2008, an Appeal Brief was filed on 8/13/09, and Examiner's Answer was filed on 11/25/2009.

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I. REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 16215 Alton Parkway, Irvine California 92618-3616, has acquired the entire right, title, and interest in and to the invention, the application, and any and all patents to be obtained therefore, as set forth in the Assignment filed with the present application and recorded on February 25, 2009 at Reel 014002 Frame 0814.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being obvious from U.S. Patent 5,903,311 to Ozcelik ("Ozcelik") in view of U.S. Patent 6,130,963 to Uz ("Uz").

Claim 6 was rejected under 35 U.S.C. 103(a) as being obvious from U.S. Patent 5,903,311 to Ozcelik in view of Uz and further in view of U.S. Patent 6,130,963 to Luna ("Luna").

Claims 7-12 were rejected under 35 U.S.C. 103(a) as being obvious from Ozcelik in view of Uz.

Claims 13 and 14 were rejected under 35 U.S.C. 103(a) as being obvious from Ozcelik in view of Uz and in further view of Luna.

Claim 15 was rejected under 35 U.S.C. 103(a) as being obvious from Ozcelik in view of Uz.

Claims 16 and 17 were rejected under 35 U.S.C. 103(a) as being obvious from Ozcelik in view of Uz and in further view of Luna.

Claim 18 was rejected under 35 U.S.C. 102(b) as being anticipated by Ozcelik.

Claim 19 was rejected under 35 U.S.C. 103(a) as being obvious by Ozcelik.

Claim 20 was rejected under 35 U.S.C. 102(b) as being anticipated by Ozcelik.

Claim 21 was rejected under 35 U.S.C. 103(a) as being as being obvious from Ozcelik.

Claims 22 and 23 were rejected under 35 U.S.C. 102(b) as being anticipated by Ozcelik.

The rejections of claims 1, 2, 7, 8, 13, 14, and 18 are appealed.

IV. STATUS OF AMENDMENTS

There are no amendments pending in the present application.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is directed to a method for displaying progressive frames, said method comprising: displaying a first portion of a progressive frame; and writing a second portion of the progressive frame while displaying the first portion of the progressive frame.

Several embodiments of claim 1 are described in the specification, for example:

(1) Claim 1 is described in the specification, for example, the specification, Figure 5A, 0049-0054 describes displaying progressive frames (0049 "There is illustrated a block diagram of an exemplary decoded progressive frame 105." See also, Figure 5A, shown below).

Displaying progressive frames comprises displaying a first portion (Figure 5A, 105a) of a progressive frame (0052, "After decoder 245 decodes portion 105a and writes portion 105a into the top region of 270(1)(c) [Figure 3], the display engine displays portion 105a.)".

The specification also describes writing a second portion of the progressive frame (for example, portion 105b) while displaying the first portion of the progressive frame (portion 105a) (0053 - "While the display engine 250 displays portion 105a, the decoder can decode portion 105b and write portion 105b to bottom region 270(2)(c).").

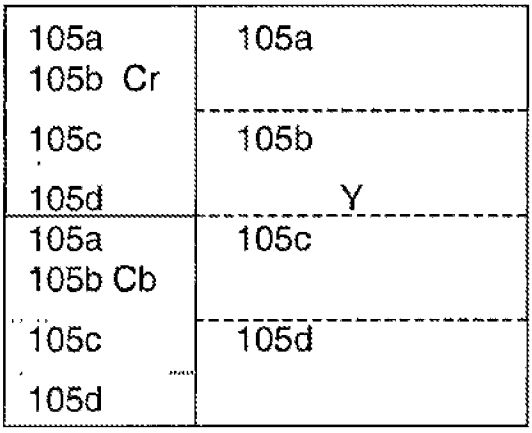

FIGURE 5A

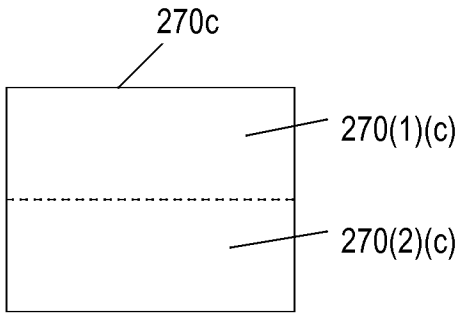

FIGURE 3
(Portion, Formalized)

(2) (First Portion 105b, Second Portion 105c) Another embodiment of claim 1 is also described in the specification.

The specification Figure 5A, 0049-0054 describes displaying progressive frames (0049 "There is illustrated a block diagram of an exemplary decoded progressive frame 105." See also, Figure 5A, shown below).

Additionally, the specification discloses displaying progressive frames comprises displaying a first portion (Figure 5A, 105b) of a progressive frame (0053, "the display engine 250 displays portion 105b").

Additionally, the specification describes writing a second portion of the progressive frame (for example, portion 105c) while displaying the first portion of the progressive frame (portion 105b) (0053 - "While the display engine 250 displays portion 105b, the decoder can decode portion 105c and overwrite portion 105a in region
270(1)(c).").

(3) (First Portion 105c, Second Portion 105d) Another embodiment of claim 1 is also described in the specification. The specification Figure 5A, 0049-0054 describes displaying progressive frames (0049 "There is illustrated a block diagram of an exemplary decoded progressive frame 105." See also, Figure 5A, shown below).

Additionally, the specification discloses displaying progressive frames comprises displaying a first portion (Figure 5A, 105c) of a progressive frame (0052, "After decoder 245 decodes portion 105c and writes portion 105c into the top region of 270(1)(c) [Figure 3], the display engine displays portion 105c.)".

Additionally, the specification describes writing a second portion of the progressive frame (for example, portion 105d) while displaying the first portion of the progressive frame (portion 105c) (0053 - "While the display engine 250

displays portion 105c, the decoder can decode portion 105d and overwrite portion 105b in region 270(2)(c).").

Claim 2 is directed to the method of claim 1, wherein writing the second portion of the progressive frame further comprises overwriting a third portion of the progressive frame with the second portion of the progressive frame.

The specification describes writing the second portion of the frame 105c/105d further comprises overwriting a third portion 105a/105b of the frame with the second portion of the frame (if claim 1 is embodiment 2, "While the display engine 250 displays portion 105b from region 270(2)(c), the decoder 245 can decode portion 105c and overwrite portion 105a in region 270(1)c)" - first portion 105b, second portion 105c, third portion 105a; if claim 1 is embodiment 3, 0053 - "While the display engine 250 displays portion 105c, the decoder can decode portion 105d and overwrite portion 105b in region 270(1)(2)" - first portion 105c, second portion 105d, third portion 105b).

Claim 7 is directed to a circuit for displaying progressive frames. The circuit comprises a memory, a display engine, and a controller. The memory stores a first portion of a progressive frame. The display engine displays the first portion of the progressive frame. The controller writes a second portion of the progressive frame in the memory, while the display engine displays the first portion.

Several Embodiments of claim 7 are described in the specification:

(1) Claim 7 is described in the specification, for example, the specification, for example, Figure 2 and

Figure 5A, 0049-0054 describe a circuit displaying progressive frames (Figure 2, generally, 0049 "There is illustrated a block diagram of an exemplary decoded progressive frame 105." See also, Figure 5A). The circuit comprises a memory (Figure 2, frame buffers 270), a display engine (Figure 2, Display Engine 350) and a controller (MPEG Video Decoder 345).

The memory (Figure 3, 270c) stores a first portion of a progressive frame (0052 "After the decoder 245 decodes portion 105a and writes portion 105a into the top region of 270(1)(c)...").

The display engine displays progressive frames comprises displaying a first portion (Figure 5A, 105a) of a progressive frame (0052, "After decoder 245 decodes portion 105a and writes portion 105a into the top region of 270(1)(c) [Figure 3], the display engine displays portion 105a.)".

The controller writes a second portion of the progressive frame (for example, portion 105b) while the display engine displays the first portion of the progressive frame (portion 105a) ("While the display engine 250 displays portion 105a, the decoder can decoded portion 105b and write portion 105b to bottom region 270(2)(c).").

(2) First Portion 105b, Second Portion 105c

(3) First Portion 105c, Second Portion 105d

Claim 8 is directed to the circuit of claim 7 wherein the controller overwrites a third portion of the progressive frame with the second portion of the progressive frame.

The specification describes the controller overwrites overwrites a third portion 105a/105b of the progressive frame with the second portion 105(c)/105d of the progressive frame (if claim 7 is embodiment 2, "While the display engine 250 displays portion 105b from region 270(2)(c), the decoder 245

can decode portion 105c and overwrite portion 105a in region 270(1)c)" - first portion 105b, second portion 105c, third portion 105a; if claim 7 is embodiment 3, 0053 - "While the display engine 250 displays portion 105c, the decoder can decode portion 105d and overwrite portion 105b in region 270(1)(2)" - first portion 105c, second portion 105d, third portion 105b).

Claim 13 is directed to the circuit of claim 12, wherein the memory comprises no more than 4 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise high definition television progressive frames with at least 1280x720 resolution.

Claim 13 is directed to the circuit of claim 12 (first prediction buffer, 270a, second prediction frame buffer 270b, delta frame buffer 270c), wherein the memory comprises no more than 4 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise high definition television progressive frames with at least 1280x720 resolution [0044] .

Claim 14 is directed to the circuit of claim 13, wherein the memory comprises no more than 8 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise high definition television progressive frames with at least 1920x1080 resolution.

Claim 14 is directed to the circuit, wherein the memory comprises no more than 4 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise high

definition television progressive frames with at least 1920x1080 resolution [0042].

Claim 15 is directed to an integrated circuit. The integrated circuit comprises a first prediction buffer, a second prediction buffer, and a delta frame buffer. The first prediction frame buffer stores a first frame. The second prediction frame buffer stores a second frame. The delta frame buffer stores a portion of a third frame.

Claim 15 is described in the specification, for example, specification 0070 and Figure 3. The specification describes an integrated circuit [0070] . The integrated circuit comprises a first prediction buffer (Figure 3, 270a), a second prediction buffer (270b), and a delta frame buffer (270c). The first prediction frame buffer stores a first frame (0041). The second prediction frame buffer stores a second frame (0041). The delta frame buffer stores a portion of a third frame (0042).

Claim 18 is directed to a circuit for displaying interlaced frames. The circuit comprises a memory, a display engine, and a controller. The memory stores a first portion of a field. The display engine displays the first portion of the field. The controller writes a second portion of the field in the memory, while the display engine displays the first portion of the field.

Claim 18 is described in the specification, for example, Figure 2 describes a circuit for displaying interlaced frames (Figure 5B, 105(0), 105(1)).

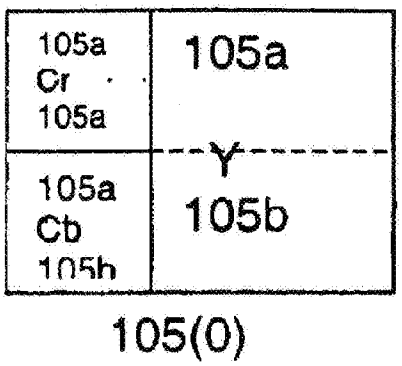

FIGURE 5A

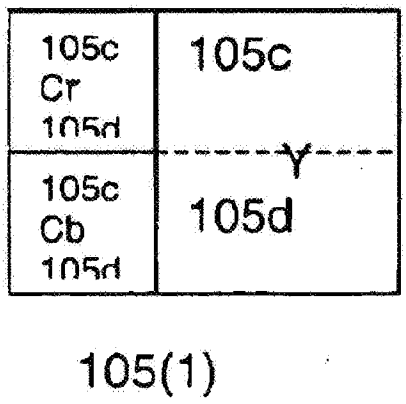

FIGURE 5B

The memory stores a first portion of a field (0057 - "In the case of an interlaced frame, the first portion can comprise the first n/64 rows of macroblocks 108 in the top field 105(0))", in connection with 0052 "After the decoder 245 decodes portion 105a and writes portion 105a into the top region of 270(1)(c)...").

The display engine displays the first portion of the field (0057 - "In the case of an interlaced frame, the first portion can comprise the first n/64 rows of macroblocks 108 in the top field" in connection with 0052, "After the decoder 245 decodes portion 105a and writes portion 105a into the top region of 270(1)(c), the display engine 250 displays portion 105a").

The controller writes a second portion of the field in the memory, while the display engine displays the first portion of the field (0057 - "The second portion 105b can comprises the remaining macroblocks 108 of the top field 105(0)" in connection with 0053, "While the display engine 250 displays portion 105a, the decoder can decode portion 105b and write portion 105b to bottom region 270(2)(c).").

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1, 2, 7, and 8 are obvious from Ozcelik in view of Uz.

Whether claims 13 and 14 are obvious from Ozcelik in view of Uz, and further in view of Luna.

Whether claim 18 is anticipated by Ozcelik.

VII. ARGUMENT: THE REJECTION TO CLAIMS 1 AND 7 SHOULD BE REVERSED BECAUSE OZCELIK AND UZ CANNOT BE COMBINED TO RESULT IN ALL OF THE LIMITATIONS OF CLAIMS 1 AND 7

Claim 1 is reproduced below:

> 1. A method for displaying progressive frames, said method comprising:
> displaying a first portion of a progressive frame; and
> writing a second portion of the progressive frame while displaying the first portion of the progressive frame.

Claim 7 is reproduced below:

> A circuit for displaying progressive frames, said circuit comprising:
> a memory for storing a first portion of a progressive frame;
> a display engine for displaying the first portion of the progressive frame; and
> a controller for writing a second portion of the progressive frame in the memory, while the display engine displays the first portion.

It appears to be Examiner's position in the Answer at 15-16 that as long as the limitations are known in the art, and that one of the references states some motivation ("efficiently displaying high quality progressive video images while reducing noise", also argued as a predictable

result), the claim is *conclusively* obvious, relying on *In re Fine*, and *In re Jones*. This is legal error.

Examiner argues that:

> "Since the concept of using fields as taught in Ozcelik can be implemented, as disclosed in Oxcelik column 12, lines 19-41, the concept of using progressive frames can be applied as taught in Uz, since it is well known in the art that a frame comprises of two fields, and the concept of progressive frames is well known in the art … Thus the teaching of Uz can be combined with Ozcelik because both Ozcelik and Uz pertain to the same video image processing environment."

Appellant respectfully submits that the above conclusion is in error. As an initial matter, "since it is well known in the art that a frame comprises of two fields" is not entirely accurate. Only interlaced frames include fields; *progressive frames* do not include fields. It is noted that Uz, which is cited for use of progressive frames, never discloses the progressive frames as including a top field and a bottom field.

Although *Fine*, and *Jones* (which were overruled in part by *KSR v. Teleflex*) held that "obviousness can only by established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one or ordinary skill in the art", neither case held that doing so *conclusively* established obviousness.

As noted in MPEP 2141:

> Office personnel should consider all rebuttal evidence that is timely presented by the applicants when reevaluating any obviousness determination. Rebuttal evidence may include evidence of "secondary considerations," such as "commercial success, long felt but unsolved needs, [and] failure of others"*(Graham v. John Deere Co.*, 383 U.S. at 17, 148 USPQ at 467), and may also include evidence of unexpected results. As set forth above, Office personnel must articulate findings of fact that support the rationale relied upon in an obviousness rejection. As a result, applicants are likely to submit evidence to rebut the fact finding made by Office personnel. For example, in the case of a claim to a combination, applicants may submit evidence or argument to demonstrate that:
>
> (A) one of ordinary skill in the art could not have combined the claimed elements by known methods (e.g., due to technological difficulties);
>
> (B) the elements in combination do not merely perform the function that each element performs separately; or
>
> (C) the results of the claimed combination were unexpected.
>
> Once the applicant has presented rebuttal evidence, Office personnel should reconsider any initial obviousness determination in view of the entire record. See e.g., *In re Piasecki*, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); *In re Eli Lilly & Co.*, 90 F.2d 943, 945, 14 USPQ2d 1741, 1743 (Fed. Cir. 1990). All the rejections of record and proposed rejections and their bases should be reviewed to confirm their continued viability."

In the present case, Appellant presented rebuttal arguments. Appellant argued that if the interlaced frames in Ozcelik were modified with the progressive frames of Uz, there would be no fields.

Reviewing Examiner's rejetion below:

A method for displaying progressive frames, said method comprising:	Ozcelik discloses a method for displaying frames, said method comprising: FOA at 5.
displaying a first portion of a progressive frame; and	displaying a first portion of a frame (col. 12, ln 19-34; Ozcelik discloses that the first portion, ie. **top field, is displayed for a frame**); FOA at 5.
writing a second portion of the progressive frame while displaying the first portion of the progressive frame.	Ozcelik discloses the second portion, **bottom field, of the frame is written buffered for storage while the first portion, ie., top field, is displayed.** FOA at 5. Uz teaches the displaying of progressive frames.

As can be seen, since progressive frames do not include top fields or bottom fields, it would be *impossible* to modify Ozcelik to include progressive frames, and yet "disclose that the first portion, i.e., *top field*, is displayed for a frame" and "the second portion, *bottom field*, of the frame is written buffered for storage while the first portion, i.e., top field, is displayed". Examiner's Answer does not even address or even consider this matter. Rather, Examiner only reiterates that each were known in the art and are therefore combinable.

Finally, Examiner asserts that "the test for obviousness is not whether the features of a secondary reference may be

bodily incorporated into the structure of the primary reference. See *In re Keller*." Answer at 17. Keller held that "To justify combining reference teachings in support of a rejection it is not necessary that a device shown in one reference can be physically inserted into the device shown in in the other. *In re Griver, 53 CCPA 815, 354 F.2d 377, 148 USPQ 197 (1966); In re Billingsley, 47 CCPA 1108, 279 F.2d 689, 126 USPQ 370 (1960)*."

The foregoing cases merely dealt with circumstances wherein a mechanical element of a secondary reference was not made to fit into a mechanical element of the primary reference. The courts reasoned that although the former could not fit into the latter, the former or the latter could easily be adapted to fit ("Naturally the shape of the groove would be adapted to that of the rib in which it is located." *In re Griver)*.

However, in the present case, Ozcelik cannot not be modified with Uz, and yet still perform the method limitation of "writing a second portion of the progressive frame while displaying the first portion of the progressive frame." In Ozcelik, the top and bottom fields are captured at different times and are received as separate units, e.g., all of the top field (even numbered lines), followed by all of the bottom field (odd numbered lines), or vice versa. For example, at:

T=0 display lines 0, 2, 4, 6, etc.; and

T=1 display lines 1, 3, 5, 7, etc.

Since the fields are displayed during different display

periods, it is possible to display one field while decoding the second field. In contrast, a progressive frame is captured and received as a single unit. The even and odd numbered lines would are displayed during the same display period, e.g., at T=0, display lines 0, 1, 2, 3, ….

As can be seen from the foregoing, Ozcelik cannot be modified to decode and display a part of the same progressive frame, using methods known to those of ordinary skill in the art.

Accordingly, the rejection should be REVERSED.

VIII. ARGUMENT: THE REJECTION TO CLAIMS 2 AND 8 SHOULD BE REVERSED BECAUSE NEITHER OZCELIK OR UZ TEACH "OVERWRITING THE THIRD PORTION OF THE ... FRAME WITH THE SECOND PORTION"

Claims 2 and 8 are reproduced below:

> 2. The method of claim 1, wherein writing the second portion of the progressive frame further comprises:
> overwriting a third portion of the progressive frame with the second portion of the progressive frame.

> 8. The circuit of claim 7, wherein the controller overwrites a third portion of the progressive frame with the second portion of the progressive frame in the memory.

Examiner's Answer at 18-19 merely reiterate the arguments presented in the Final Office Action. Examiner fails to address the fact that "implementation of first second ,third, fourth, fifth or more sections for storimg

multiple sections or portions of image data" and "overwriting" teach, the specifically claimed, "*overwriting a third portion of the progressive frame with the second portion of the progressive frame*".

Appellant respectfully submits that merely teaching overwriting and use of first, second, and third portions of the frame, does not teach overwriting the *third portion* with the *second portion*.

In fact, if as Examiner asserts, "Ozcelik permits 'use of first, second, third, fourth, fifth or more sections for storing multiple sections or portions of image data'", it would follow that Ozcelik would not overwrite the one of the "first, second, third, fourth, fifth or more portions of a frame" with another of the first, second, third, fourth, fifth or more portions of a frame. The purpose of the first, second, third, fourth, fifth or more sections would be to precisely avoid this.

Accordingly, Assignee respectfully submits that the rejection to claims 2 and 8 should be REVERSED because the combination of Ozcelik and Uz does not teach all of the limitations of claims 2 and 8.

IX. ARGUMENT: THE REJECTIONS TO CLAIMS 13 AND 14 SHOULD BE REVERSED THE PROPOSED COMBINATION OF OZCELIK AND UZ COULD NOT BE COMBINED WITH LUNA TO TEACH THE LIMITATIONS OF CLAIMS 13 AND 14.

Claims 13 and 14 are reproduced below:

13. The circuit of claim 12, wherein the memory comprises no more than 4 megabytes, and wherein the

progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise high definition television progressive frames with at least 1280x720 resolution.

14. The circuit of claim 13, wherein the memory comprises no more than 8 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise high definition television progressive frames with at least 1920x1080 resolution.

Again, it appears to be Examiner's position in the Answer at 20-21 that as long as the limitations are known in the art, and that one of the references states some motivation, the claim is *conclusively* obvious, relying on *In re Fine*, and *In re Jones*. This is legal error.

Again, Appellant calls attention to MPEP 2141, in particular, consideration of argument/evidence that "one of ordinary skill in the art could not have combined the claimed elements by known methods (e.g., due to technological difficulties)".

Assignee respectfully submits that the foregoing is in error because if Ozcelik and Uz were modified to use high definition television, it would no longer be the case that "3 megabytes is needed for buffering the frame data". It is noted that Ozcelik uses standard NTSC size frames of 720x480 pixels. See Col. 4, Line 41. Clearly when higher resolution frames are used, e.g., 1280x720 (approximately 2.66 times more pixels), or 1920x1080 (six times more pixels), more memory is required. If Ozcelik/Uz are modified to include Luna's 1280x720 pixels or 1920x1080 pixels, 2.66 or 6 times

more memory would be required.

Finally, Examiner asserts that "the test for obviousness is not whether the features of a secondary reference may be *bodily* incorporated into the structure of the primary reference. See *In re Keller*." Answer at 21. Keller held that "To justify combining reference teachings in support of a rejection it is not necessary that a device shown in one reference can be physically inserted into the device shown in in the other. *In re Griver, 53 CCPA 815, 354 F.2d 377, 148 USPQ 197 (1966); In re Billingsley, 47 CCPA 1108, 279 F.2d 689, 126 USPQ 370 (1960)*."

The foregoing cases merely dealt with circumstances wherein a mechanical element of a secondary reference was not made to fit into a mechanical element of the primary reference. The courts reasoned that although the former could not fit into the latter, the former or the latter could easily be adapted to fit ("Naturally the shape of the groove would be adapted to that of the rib in which it is located." *In re Griver)*.

Clearly, in the present case, Ozcelik/Uz cannot be modified by using methods known by those skilled in the art to use HDTV frames while staying within the memory confines of the claimed limitations.

Accordingly, Appellant respectfully requests the rejections to claims 13 and 14 be REVERSED.

X. ARGUMENT: THE REJECTION TO CLAIM 18 SHOULD BE REVERSED BECAUSE OZCELIK DOES NOT TEACH ALL OF THE LIMITATIONS

Claim 18 is reproduced below:

> A circuit for displaying interlaced frames, said circuit comprising:
> a memory for storing a first portion of a field;
> a display engine for displaying the first portion of the field; and
> a controller for writing a second portion of the field in the memory, while the display engine displays the first portion of the field.

Appellant respectfully submits that the rejection to claim 18 is in error because Ozcelick does not teach "a controller for writing a second portion of the field in the memory, while the display engine displays the first portion of the field".

Examiner has responded by pointing out that:

> Ozcelik discloses the second portion, ie. Bottom field, of the frame is written or buffered for storage while the first portion, i.e., top field, is displayed, in that the first portion of the top field is displayed in that the top field displayed requires some buffering, thus, the display of the top field does display the first portion of the top field, and while buffering the second portion of the top field during the display of the top field, thus the second portion of the field is written in the memory while the first portion if field is displayed.

The foregoing argument by Examiner still fails to establish "a controller for writing a *second portion of the field* in the memory, while the display engine displays the *first portion of the field*". It is first noted that, due to antecedent basis, the first portion and second portion must

be of the *same* field.

First, Examiner states "**second** portion, ie. ***Bottom*** field, of the frame is written or buffered for storage while the **first** portion, i.e., ***top*** field, is displayed". This does not establish the foregoing limitation, because the fields are different, e.g., top and bottom.

Next, Examiner states, "while the **first** portion, i.e., **top** field, is displayed, in that the **first** portion of the **top** field is displayed in that the ***top*** *field* displayed requires some buffering, thus, the display of the **top** field does display the ***first*** *portion of the* ***top*** *field*, and while buffering the ***second*** *portion of the* ***top*** *field* during the display of the **top** field".

However, even if the **second** portion of the **top** field is buffered, during display of the **first** portion of the **top** field, it does not follow that the **second** portion of the **top** field is *written* during display of the **first** portion of the **top** field. For example, the **entire top** field may be have been written to the memory at substantially the same time, and prior to display of any portion of the top field.

Finally, Examiner concludes that "thus the second portion of the field is written in the memory while the first portion if field is displayed". The conclusion does not follow. It appears to be Examiner's reasoning that since:

(1) a field is written and buffered while a *different* field is displayed; and
(2) a portion of a field is displayed while another portion of the same field is buffered,

that it somehow follows that a portion of field is displayed while another portion of the same field is written to memory.

Assignee respectfully submits that the foregoing reasoning is in error. Accordingly, Appellant respectfully requests that the rejection to claim 18 be REVERSED.

XI. CONCLUSION

For at least the foregoing reasons, the Board of Patent Appeals and Interferences is respectfully requested to REVERSE the rejections to claims 1, 2, 7, 8, 13, 14, and 18.

The Commissioner is hereby required to charge any overpayments or additional fees to Deposit Account No. 13-0017.

Dated: January 25, 2010

Respectfully submitted,

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CLAIMS APPENDIX

CLAIM LISTING

Please amend the claims as follows:

1. A method for displaying progressive frames, said method comprising:

displaying a first portion of a progressive frame; and

writing a second portion of the progressive frame while displaying the first portion of the progressive frame.

2. The method of claim 1, wherein writing the second portion of the progressive frame further comprises:

overwriting a third portion of the progressive frame with the second portion of the progressive frame.

3. The method of claim 1, wherein writing the second portion of the progressive frame further comprises:

decoding the second portion of the progressive frame.

4. The method of claim 1, further comprising:

displaying the second portion of the progressive frame responsive to displaying the first portion of the progressive frame;

overwriting the first portion of the progressive frame with a fourth portion of the progressive frame.

5. The method of claim 1, further comprising:

displaying the second portion of the progressive frame responsive to displaying the first portion of the progressive frame; and

overwriting the first portion of the progressive frame with a first portion of another progressive frame while displaying the second portion of the progressive frame.

6. The method of claim 1, wherein the progressive frame comprises a high definition television progressive frame.

7. A circuit for displaying progressive frames, said circuit comprising:

a memory for storing a first portion of a progressive frame;

a display engine for displaying the first portion of the progressive frame; and

a controller for writing a second portion of the progressive frame in the memory, while the display engine displays the first portion.

8. The circuit of claim 7, wherein the controller overwrites a third portion of the progressive frame with the second portion of the progressive frame in the memory.

9. The circuit of claim 7, wherein the controller decodes the second portion of the progressive frame.

10. The circuit of claim 7, wherein:

the display engine displays the second portion of the progressive frame responsive to displaying the first portion of the progressive frame; and

the controller overwrites the first portion of the progressive frame with a fourth portion of the progressive frame in the memory.

11. The circuit of claim 7, wherein:

the display engine displays the second portion of the progressive frame responsive to displaying the first portion of the progressive frame; and

the controller overwrites the first portion of the progressive frame with a first portion of another progressive frame while the display engine displays the second portion of the progressive frame.

12. The circuit of claim 7, wherein the memory further comprises:

a first prediction frame buffer for storing a first prediction frame;

a second prediction frame buffer for storing a second prediction frame; and

a delta frame buffer for storing the first portion of the progressive frame and the second portion of the progressive frame.

13. The circuit of claim 12, wherein the memory comprises no more than 4 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise high definition television progressive frames with at least 1280x720 resolution.

14. The circuit of claim 13, wherein the memory comprises no more than 8 megabytes, and wherein the progressive frame and the first prediction progressive frame and the second prediction progressive frame comprise

high definition television progressive frames with at least 1920x1080 resolution.

15. An integrated circuit for storing decoded frames, said integrate circuit comprising:

a first prediction frame buffer for storing a first progressive frame;

a second prediction frame buffer for storing a second progressive frame; and

a delta frame buffer for storing a portion of a third progressive frame.

16. The integrated circuit of claim 15, wherein the integrated circuit comprises no more than 4 megabytes of memory, and wherein the first progressive frame and the second progressive frame and the third progressive frame comprise high definition television frames with at least 1280x720 resolution.

17. The integrated circuit of claim 15, wherein the integrated circuit comprises no more than 8 megabytes of memory, and wherein the first progressive frame and the second progressive frame and the third progressive frame comprise high definition television frames with at least 1920x1080 resolution.

18. A circuit for displaying interlaced frames, said circuit comprising:

a memory for storing a first portion of a field;

a display engine for displaying the first portion of the field; and

a controller for writing a second portion of the field in the memory, while the display engine displays the first portion of the field.

19. The circuit of claim 18, wherein the controller overwrites a third portion of the field with the second portion of the field in the memory.

20. The circuit of claim 18, wherein the controller decodes the second portion of the field.

21. The circuit of claim 18, wherein:

the display engine displays the second portion of the field responsive to displaying the first portion of the field; and

the controller overwrites the first portion of the field with a fourth portion of the field in the memory.

22. The circuit of claim 18, wherein:

the display engine displays the second portion of the field responsive to displaying the first portion of the field; and

the controller overwrites the first portion of the field with a first portion of another field while the display engine displays the second portion of the field.

23. The circuit of claim 18, wherein the memory further comprises:

a first prediction frame buffer for storing a first prediction frame;

a second prediction frame buffer for storing a second prediction frame; and

a delta frame buffer for storing the first portion of the field and the second portion of the field.

EVIDENCE APPENDIX

There are no pages in this Appendix.

RELATED PROCEEDINGS APPENDIX

There are no pages in this Appendix.